Constellation-X:
CCD Plans and Progress Report

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Constellation-X Technology Meeting

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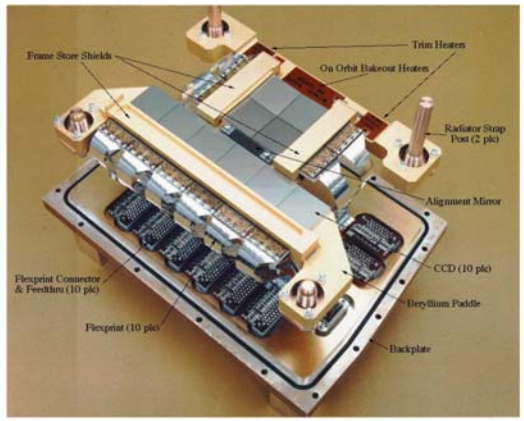
Outline

- Current Baseline: Resistive Gate CCD (RGCCD)
- Motivation for the Event-Driven CCD (EDCCD)
- Description of the EDCCD
- Implications of the EDCCD
  - Back-illuminated (BI) configuration: Improved low-energy response
  - Improved radiation hardness
- Current status and proposed program

Heritage of the *Constellation-X* CCD Camera

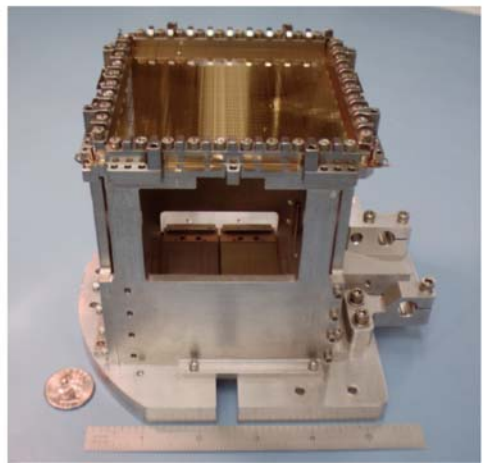
ASCA/SIS (1993)

Chandra/ACIS (1999)



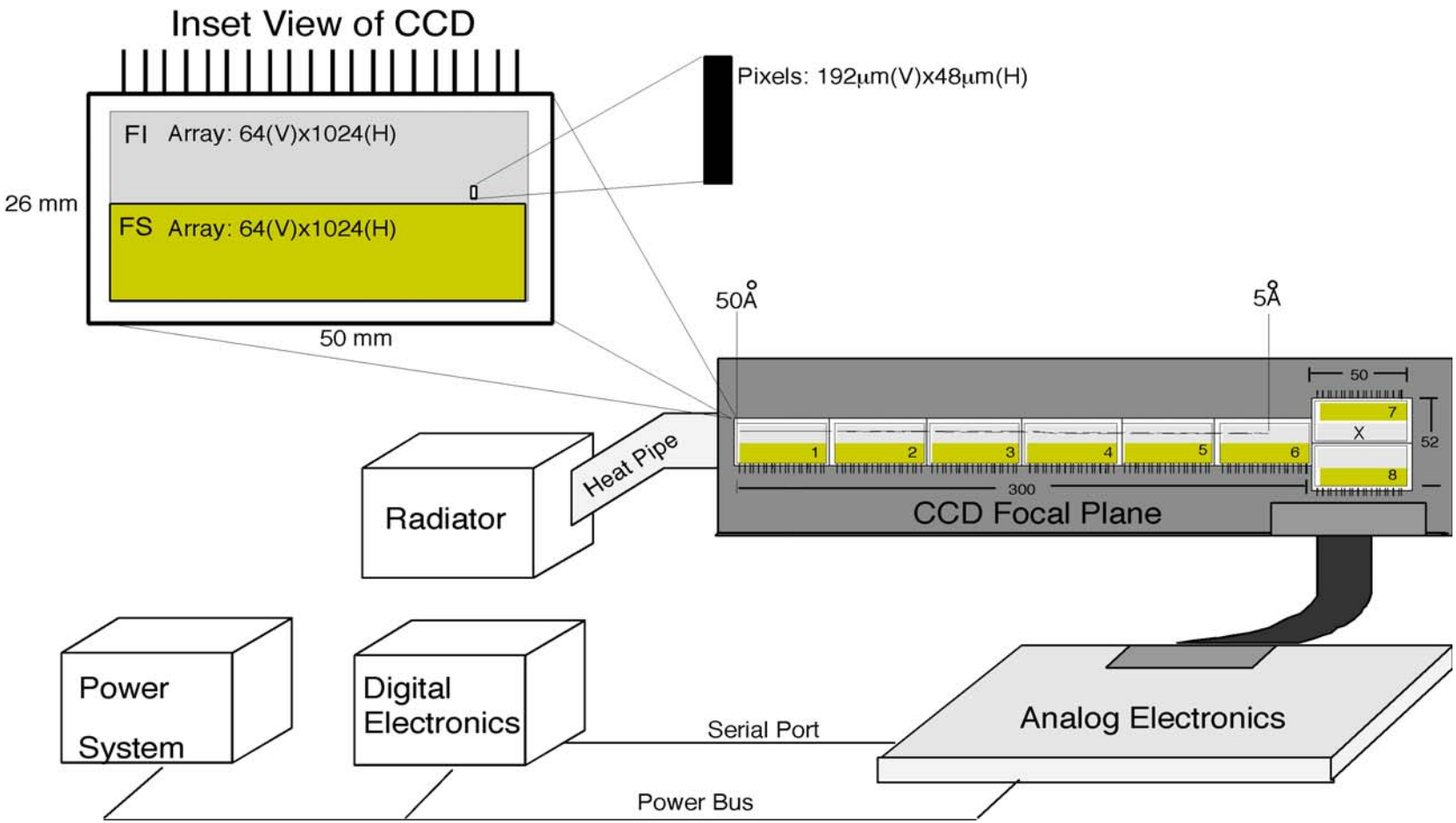
Astro-E/XIS (2000)

HETE SXC (2000)



Constellation-X RGCCD Camera Reference Design

Schematic of *Constellation-X* RGCCD Camera



Comparison: Chandra/ACIS vs Con-X/RGCCD

Parameter	*Chandra* /ACIS	*Constellation*-X
Format (Image Area)	1024 x 1024	64 x 1024
Pixel Size	24 x 24 microns	48 x 192 microns
Depletion Depth	70 microns	40 microns
Readout Noise	2-3 e^-	2-3 e^-
Array Length	150 mm	350 mm
Devices per Array	10	8
No. of Flight Arrays	1	4
Pixel Readout Rate	400 kpixels/s/device @ 0.3 Hz frame rate	655 kpixels/s/device @ 10 Hz frame rate
Operating Temperature	-120 C	-60 C
Radiation Tolerance (Relative)	3	30
Low Energy Limit	0.4 keV	0.2 keV

GOALS:

Pixel Sizes: 48 μm x 192 μm for In-Plane Grating
24μm x 24μm for Off-Plane Grating

Excellent low energy QE: equivalent to a back-illuminated (BI) device

Higher frame rates: ~ 10 frames/sec

Radiation hard: ~ 10 times harder than the Chandra devices

Higher yields: ~ 10 times higher than BI devices

Lower system electronics power: 10-20 times less than for current devices

Summary of RGCCD Status

- Test lot of RGCCDs was fabricated and tested in 1998-1999
  - –Test devices had 1/4 pixel count of flight design
  - –Devices were functional, but not optimal
  - –Energy resolution was poor
  - –Additional lots would be essential to refine the design
- Devices were (*marginally*) understood at TRL3
- No Constellation-X funds for CCD effort was allocated for 2001
  - –Grating/CCD Team funding in 2001 was entirely devoted to gratings to bring them to TRL3
- Bottom Line:
  - –*No progress was made in developing RGCCDs in 2000-2002*
  - –*No low energy tests; no radiation hardness tests; no yield info*

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  - Improved radiation hardness
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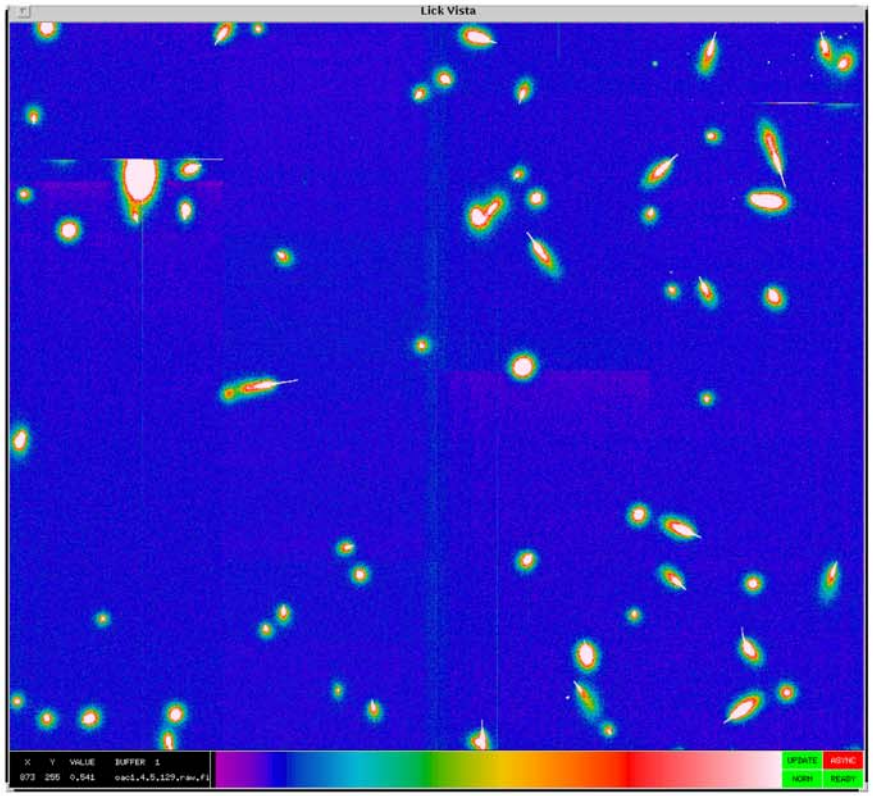
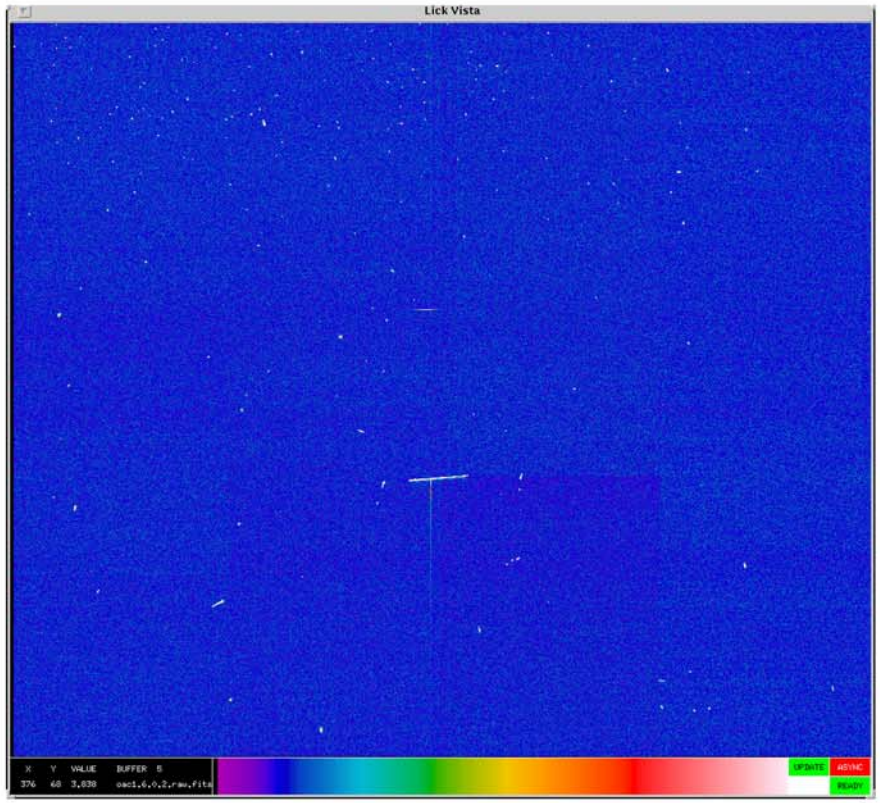
Pixels with Signal Charge are Sparse in X-ray Astronomy Images...

FI=Front-illuminated CCD S2 = w182c4r



BI=Back-illuminated CCD S3 = w134c4r



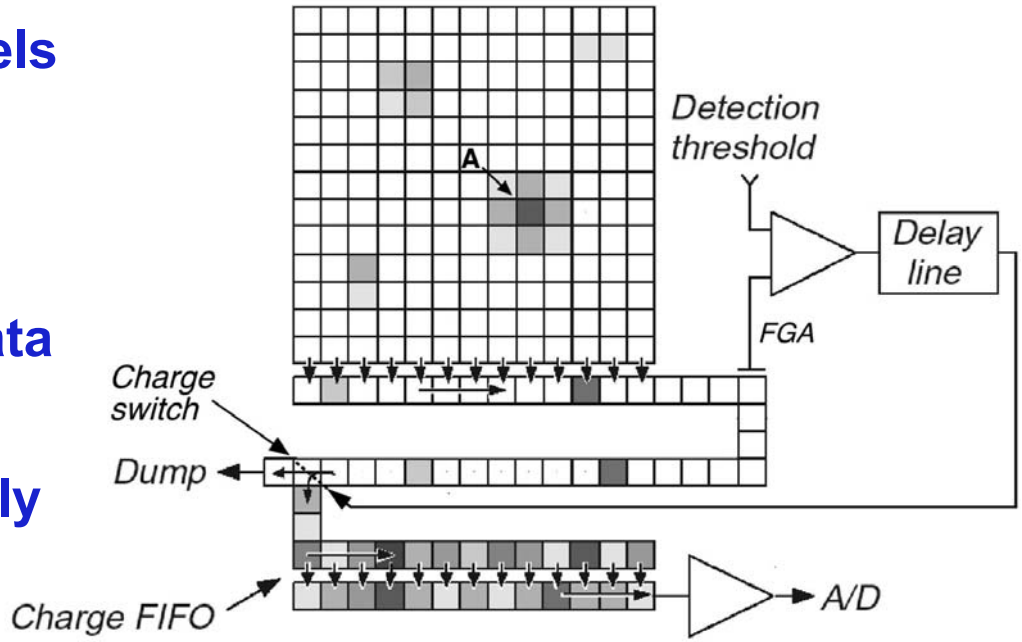
—Pixels with charge above threshold in 3.3 s exposure—

FI: 26278 out of 1,048,576 pixels = 2.5% **BI: 970 out of 1,048,576 pixels = 0.09%**

Bottom Line: ~10^{-2} to 10^{-3} of pixels contain signal charge

Event-Driven CCD

- Single photon imagery in X-ray astronomy results in sparse array utilization (< 10^{-3} of pixels have charge)
- Large power penalty for reading entire image just to examine pixels containing data
- In EDCCD, pixels are non-destructively sensed, and only those with signal charge are saved and digitized
- Novel approach (MIT patent applied for)



(Doty and Ricker 2002)

Relevance to NASA X-ray Astronomy Missions

- **EDCCD: Combines High Speed and Low Power Imager**
- **Present X-ray CCDs are extremely wasteful of power: Charge from every CCD pixel is digitized to high precision, even though less than one percent of the pixels contain useful information. The excessive use of power, in turn, limits the speed at which the pixels can be read out, as the *dissipation of heat within the analog electronics* becomes problematic.**
- **EDCCD detector responds only to pixels with charge exceeding a programmable level; only digitize a 3x3 or 5x5 pixel subarray centered on the detected pixel.**
- **X-ray EDCCDs**
  - **Operable at high speeds (>100 frames/s, thus dramatically reduced dark current per frame)**
  - **High frame rates mean greater immunity to contamination from optical and IR light (thus thinner optical blocking filters [OBFs] can be used)**
  - ***Thinner OBFs mean improved low energy X-ray response***
  - **Very low power (100x less than that of present devices)**
  - **Reduced dark current per frame means good performance near room temperature (~0 C), rather than requiring cryogenic temperatures (<-90 C) as do current devices**
  - **Utilizes flight-proven (*Astro-D, Chandra*) floating diffusion amplifier plus new low noise floating gate amplifier (developed at MIT in 2000)**
  - **Conventional parallel and serial register technologies**

Advantages of EDCCD for Con-X

- **System Constraints are relieved**
  - Lower power dissipation at a given frame rate (>100 x less)
  - Operates near room temperature (T ~ 0˚ C)
  - Reduced pileup concerns even for 5″ optics (100 frames per sec)
  - Reduced shielding requirement (>10x more radhard)
  - Relaxed S/C stability and jitter requirements
- **Improved Scientific Performance**
  - Compatible with high yield back-illuminated (MBE) approach
  - Uses thinner optical blocking filter (OBF), since has *5 magnitudes less susceptibility to optical/IR*
  - Improved QE for 0.1 - 1 keV band for which grating/CCD is optimum
  - Improved resolution for timing studies
  - Stability to radiation damage
  - Prospect of high yields (thus, can select near-ideal flight devices)
    - Conventional processing (cf RGCCD)
    - Compilation of separately-tested innovations

EDCCD Requires Low System Power

Power Requirements for a "Gen1" 512 x 512 Event Driven CCD

Power 3.3 V			
Focal plane power:		**Support power:**	
Clocks	5 mW	Focal plane bias generation [a]	10 mW
Comparators	4 mW	Analog chain	20 mW
Logic (FPGA)	25 mW	ADC	4 mW
Video buffers	3 mW	Digital processing (FPGA)	25 mW
	37 mW		59 mW

Grand total: 96 mW

[a] A small amount of bias power may be required at other voltages. This is a minor portion of the system power, and its generation is a minor portion of the system complexity.

Power Requirements: EDCCD vs. Chandra

System Design Characteristics	ACIS Imager	EDCCD (Gen II) Imager
Supply Voltages	±5, ±15, +24	+3.3
Frame Rate (Hz)	0.3	100
Chips	4	1
Raw Pixel Rate (MHz)	1.6	110
Output Pixel Rate (MHz)	1.6	0.1
Digitization	12 bit	12 bit
Noise	2-3 e^-	2-3 e^-
Signal Processing Energy (μJ pixel^{-1})	10	0.4
Operating Temperature (C)	-120	0
Depletion Depth (μm)	75	40 – 50
Peak Dynamic Power per Chip	**ACIS**	**EDCCD (Gen II)**
Specific Gate Capacitance, (nF cm^{-2})	5	1.5
Pixel Area (μm^2)	576	576
Format (imaging area)	1024 × 1024	1024 × 1024
Frame Store Height (pixels)	1024	512
Relative Clock Driver Loss [a]	3	0.75
Clock Swing [b]	10 V	3.3 V
Phases	3	3
Frame Store Factor [c]	2	2
Energy per frame (mJ) [d]	**56**	**0.19**
Frame Transfer Time (ms)	10	0.5
Peak Dynamic Power (W) [e]	**5.6**	**0.38**

Energy dissipation is 300 times less for EDCCD

[a] The amplifier-based ACIS drivers include adjustable regulators: these cost power. The EDCCD clock levels are not adjustable, and the switch-based EDCCD drivers recover part of the stored capacitive energy. We employed this same approach for our SIS instrument on .

[b] This factor appears as the square in the product, i.e. the energy per frame.

[c] The frame store must be clocked during frame transfer operation.

[d] Energy per frame is the product of preceding entries in each column.

[e] Peak dynamic power is energy per frame divided by frame transfer time.

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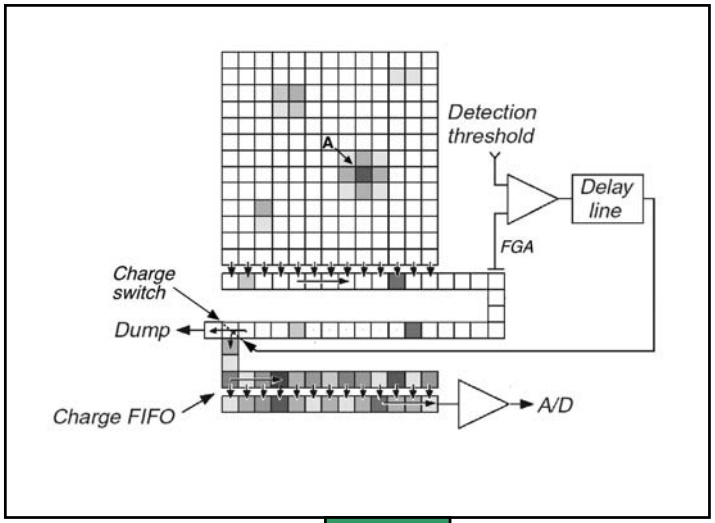
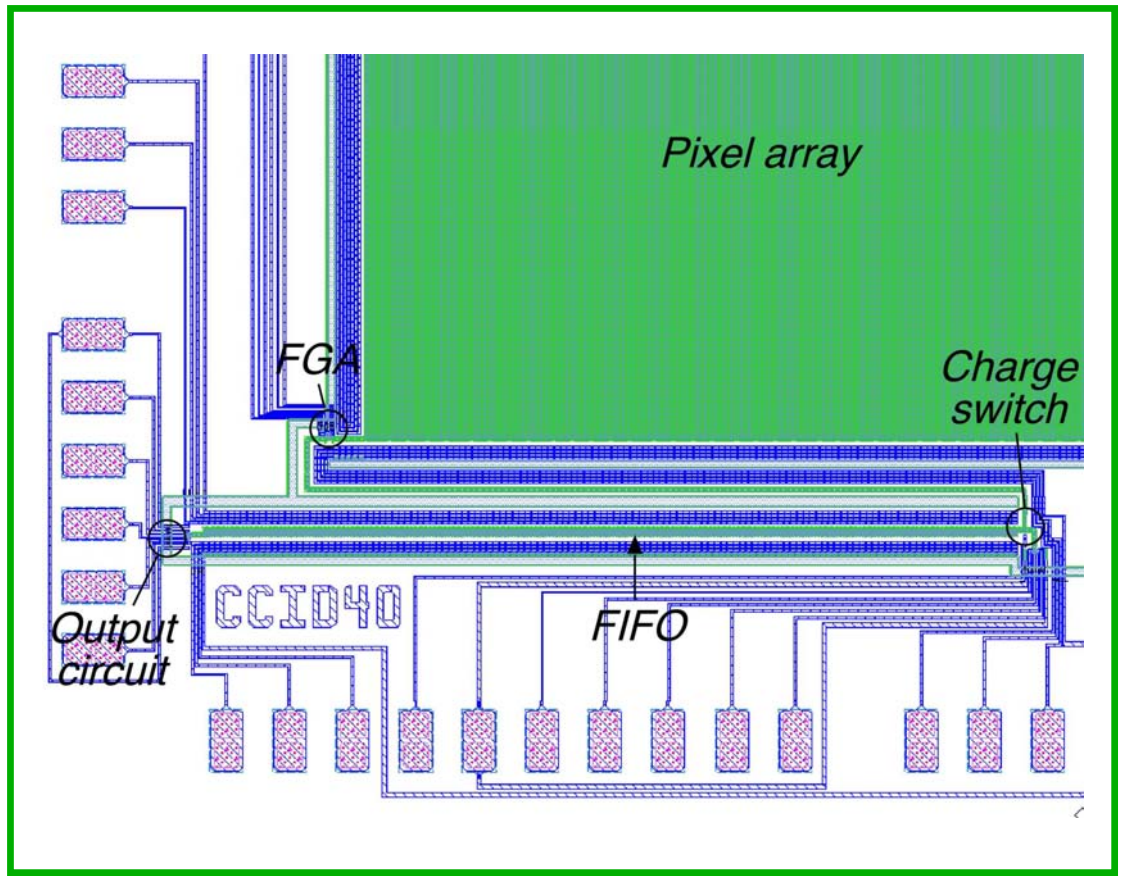
EDCCD Test Device Layout

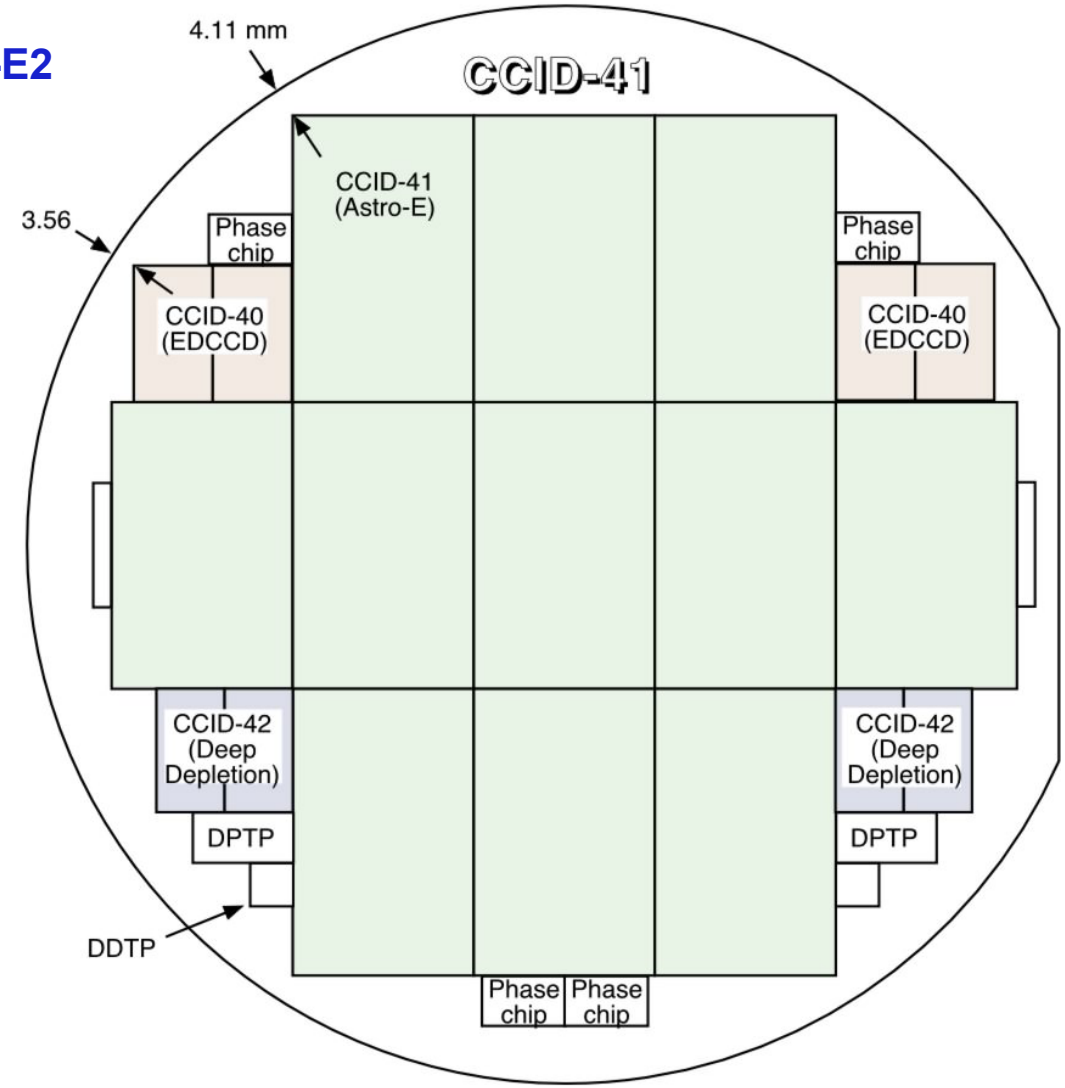
- 512 × 512-pixel device design completed 11/01





CCID-40/41/42 Wafer Layout

EDCCD Test Device Design placed on wafers for Astro-E2 program as a "piggy back" experiment



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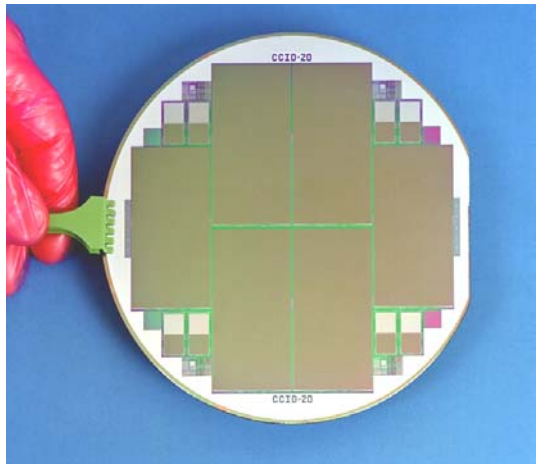
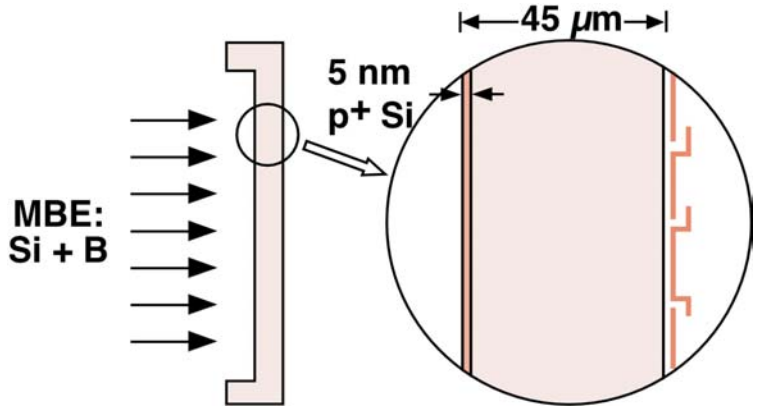
Molecular Beam Epitaxy (MBE) Back Illumination (BI) Process

- **Produces much thinner BI deadlayer:**
  - **Refractory process (ACIS): ~ 500Å**
  - **New MBE Process: ~ 50Å**
- **Yield is greatly improved:**
  - **Low temperature process (425°C vs 900°C)**
  - **Metalization is unaffected at lower temperature**
  - **Slip dislocations do not occur**
  - **Benefits from MBE developments at MIT/LL for DOD optical sensors**
- **Compatible with wafer-level thinning:**
  - **Well-developed, high yield process at MIT/LL for 6 inch wafers**
- **Backside gate can produce stronger fields to reduce charge packet recombination losses**

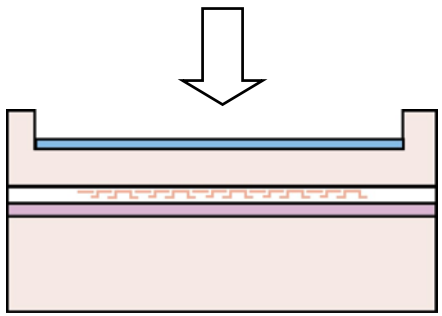
New Back-Illumination MBE Process (Developed at MIT/LL in 2000-2001)



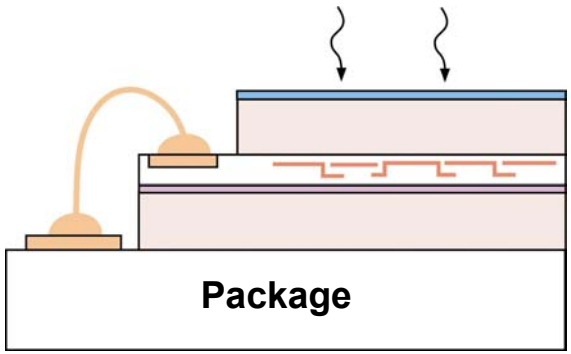
CCD wafer completed through frontside processing



Chemically thin center of wafer; grow p^+ on back surface by low temp MBE; deposit thin SiO_2 insulator and Al OBF



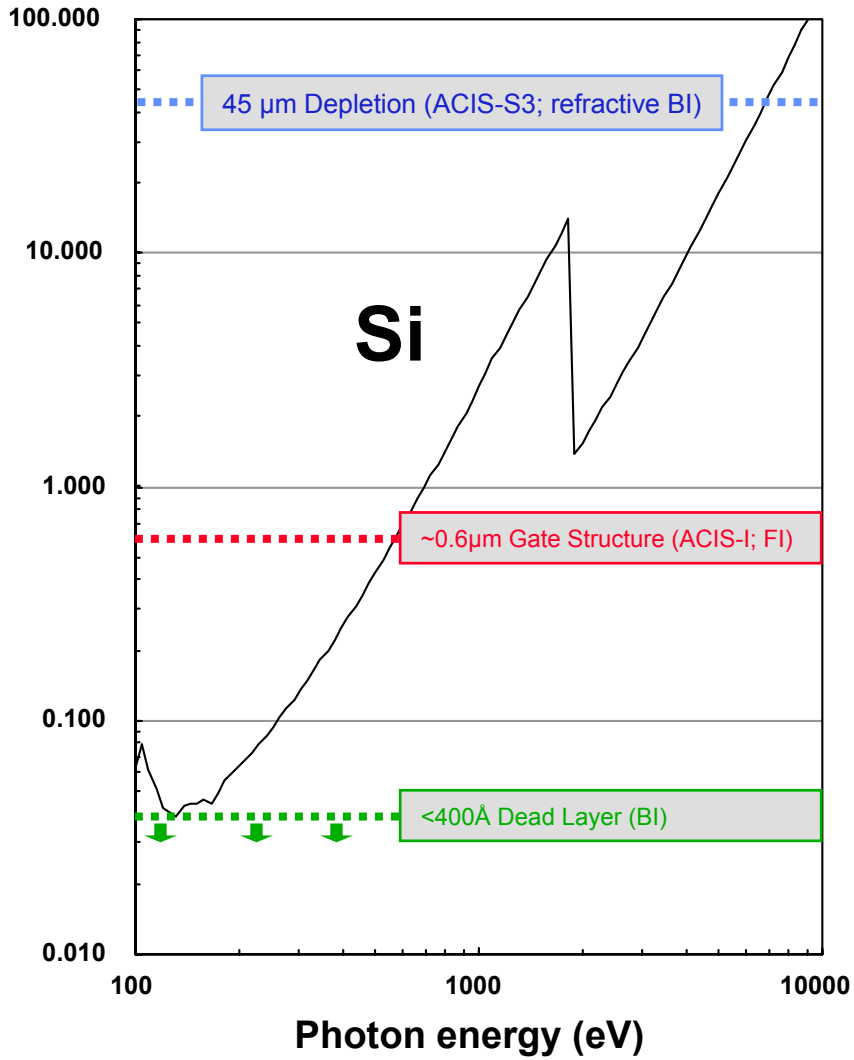
Epoxy thinned CCD to support wafer



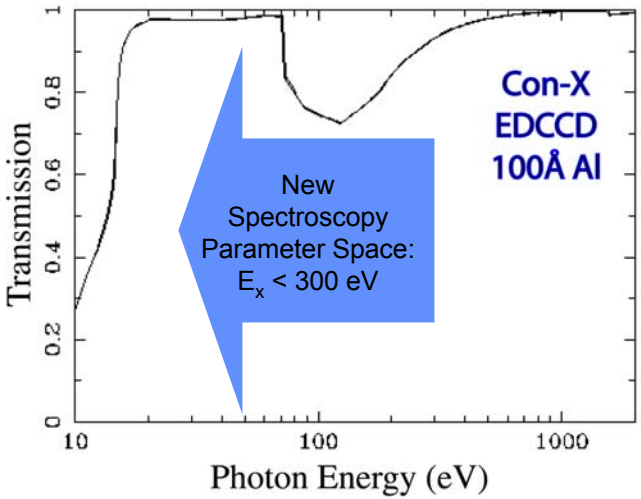
Etch to expose bond pads; saw wafer and package CCDs

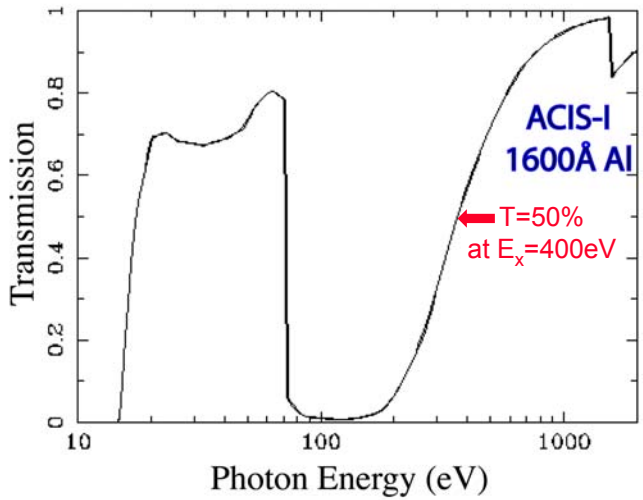
Effect of SiO_2 Deadlayer on BI CCD QE

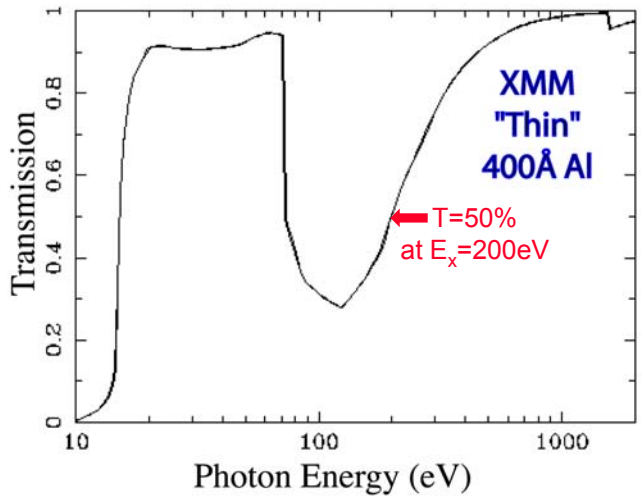
- 30µm – 40µm depletion depth suffices for Con-X to give good QE up to 3 keV
- Front-illuminated (FI; ACIS-like) device would severely limit X-ray sensitivity fo E_x < 0.5 keV
- Back-illuminated (BI) device can in principal provide good sensitivity down to E_x <~100eV
- BUT...BI devices have proven difficult to fabricate with previous CCD technologies (low yields; <0.2 % for ACIS)
- Thus, new BI technology is indicated for Con-X.

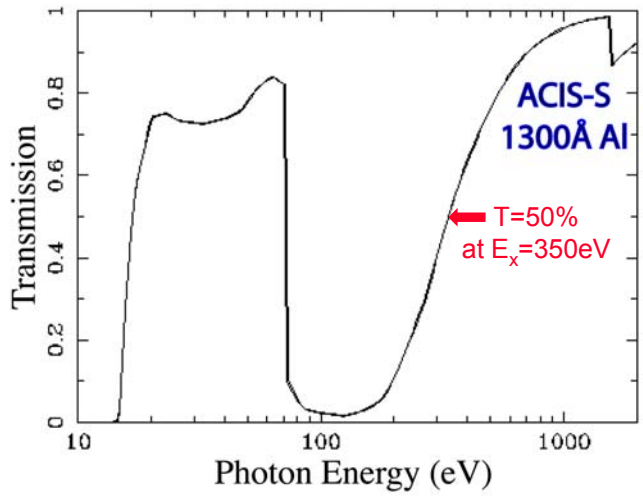


Effect of OBF's on Low Energy QE

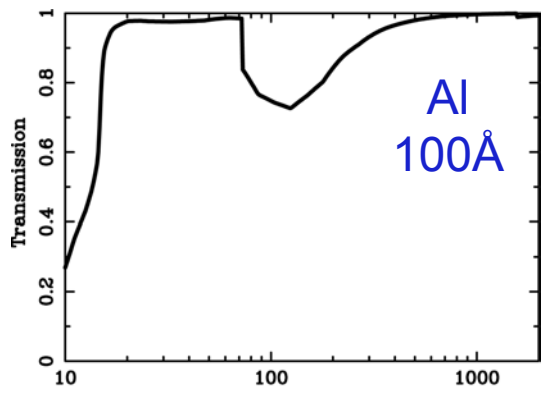


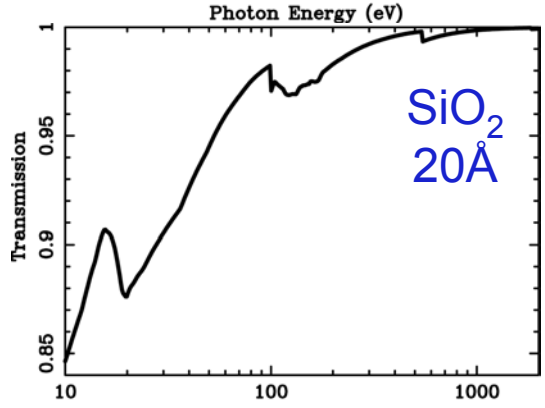


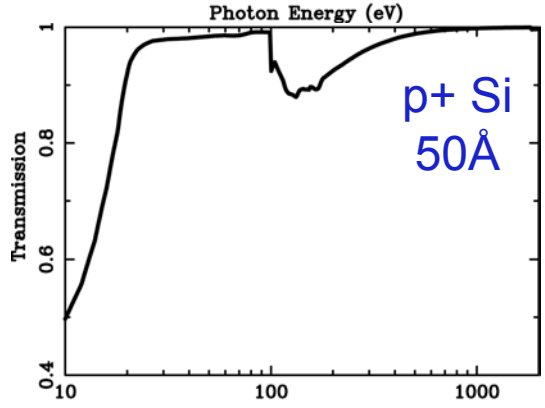




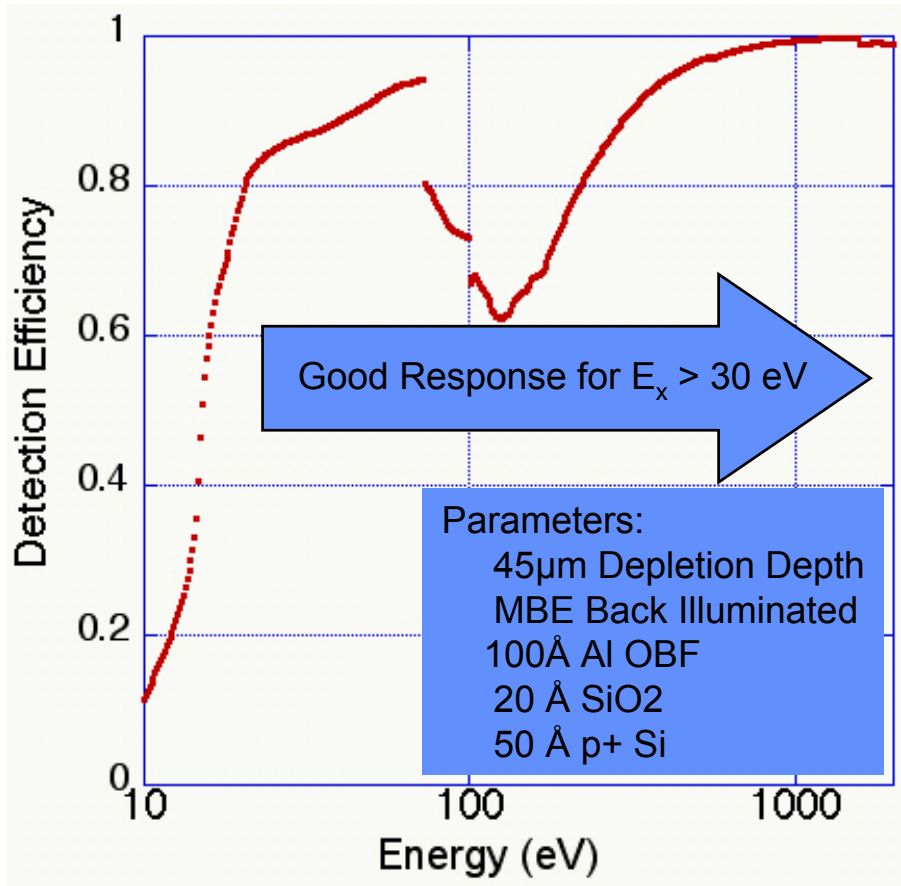
Contributions to Predicted Soft X-ray Response of an MBE/BI EDCCD for Constellation-X





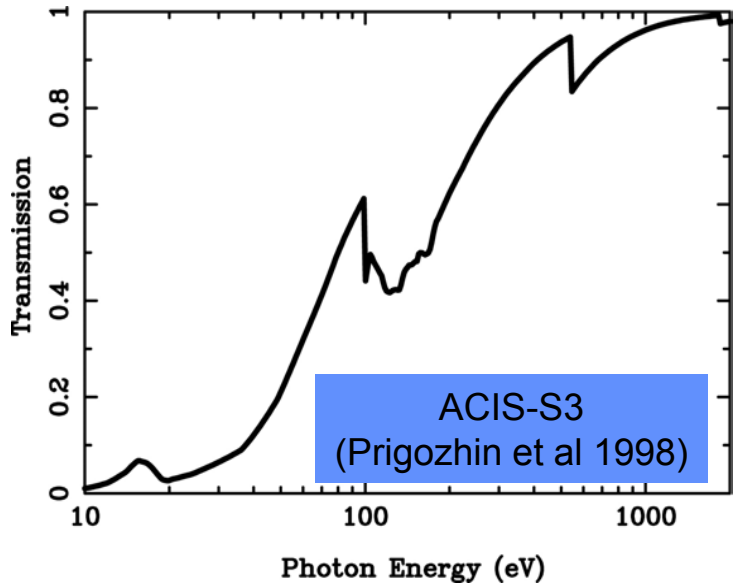


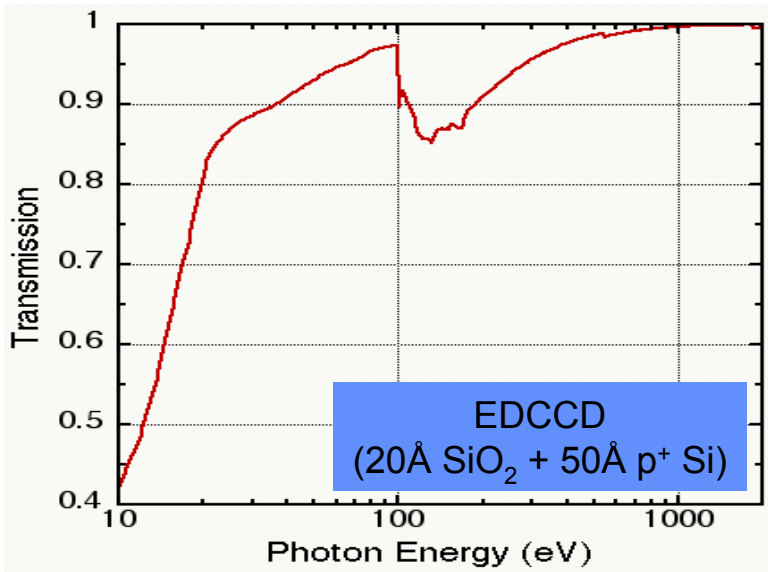
EDCCD--Predicted Low Energy Response



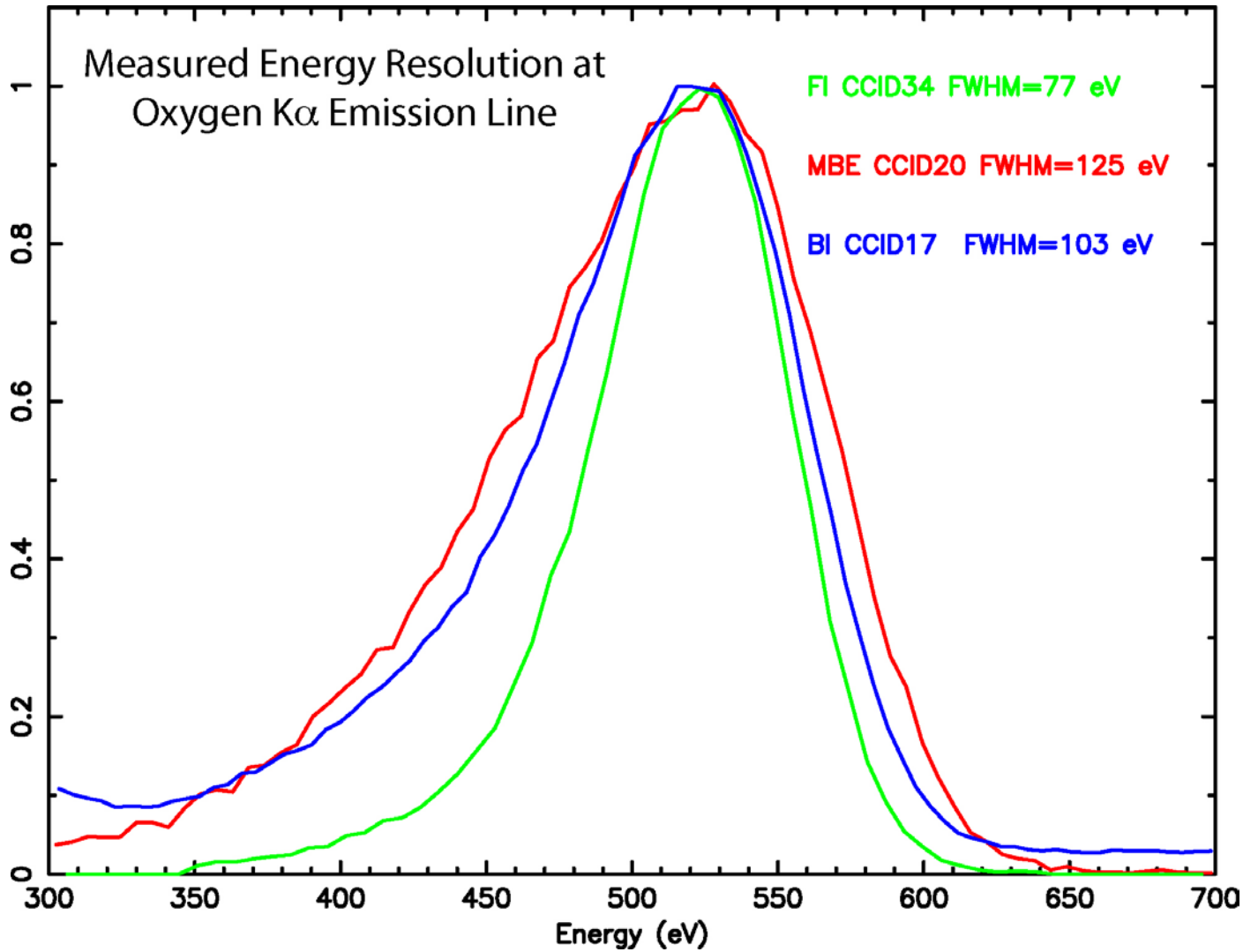
Quantum Efficiency Comparison: ACIS-S3 (BI) vs EDCCD (BI)

- Plots show QE of "bare CCD" ie no OBF
- Fact that the EDCCD can utilize >10x thinner OBF allows it to take advantage of the increased low energy QE
- Conclusion: EDCCD with MBE backside potentially can dramatically increase QE in soft X-ray band





Measured Energy Resolution at 525 eV: MBE and *Chandra* FI/BI CCDs



***Bottom Line*: Energy Resolution of MBE is already comparable to Best Previous BI CCD**

Radiation Damage in CCD Systems

- Long-term radiation damage effects in Si CCDs
  - Dark current increase
  - Charge loss due to radiation-induced traps
- Conventional remediation techniques:
  - Shielding
  - Low temperatures: suppresses dark current, traps remain filled for t >> frame period
- Drawbacks of conventional approaches:
  - Power (TECs)
  - Weight (shielding, deep-space radiator)

Radiation Hardness and High Frame Rates: Advantages of EDCCD

- Lower system power means that EDCCDs can operate at higher frame rates to reduce dark charge/frame
- Reduced dark signal allows higher device temperature
  - Thermally-generated carriers populate traps
  - Trapping times remain short compared to frame times, thus no frame-to-frame “memory” effects
  - Power and weight system savings from less demanding thermal systems
- High frame rates are advantageous for X-ray astronomy (signal amplitudes are independent of frame rate)

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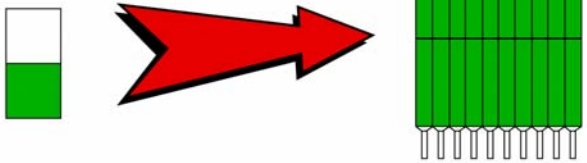
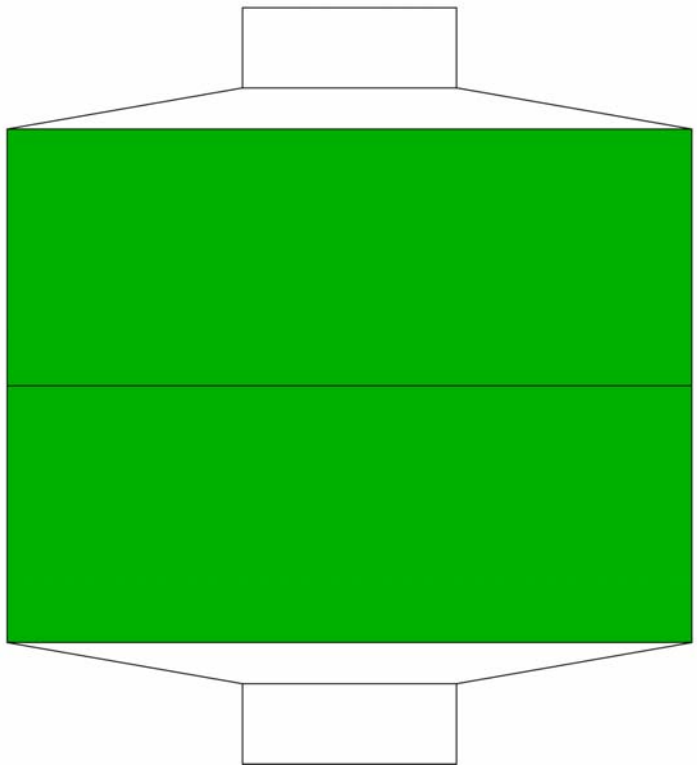
Roadmap for EDCCD Development

Generation I:
512 x 512 pixel array
pixel size: 15 x 15 μm (FI)
15 x 15 μm (FS)
Imaging area: 0.6 cm^2



Generation II:
1024 x1024 pixel array
pixel size: 24 x 24 μm (FI)
7.5 x 7.5 μm (FS)
Imaging area: 6 cm^2



FI = Imaging Frame
FS = Frame Store

Generation III:
3000 x 4000 pixel array
pixel size: 24 x 24 μm (FI)
7.5 x 7.5 μm (FS)
Imaging area: 70 cm^2

Current Status and Future Plans

- Design and CAD layout of prototype EDCCD complete
- Fabrication of Prototype "Gen 1" Device
  - Test device (CCID40; 512 x 512 array)
  - Funded by MIT internal funds and NASA ROSS2000
  - Shared lot with Astro-E2 program
  - Fabrication began 2/02; first lot completion, 7/02
  - Device packaging and preliminary screening, 8/02
- NASA Con-X Technology Funding Request for EDCCDs
  - Propose use of Con-X funds for mask design in FY02 for Gen2 EDCCD (1024 x 1024; 24μm x 24μm pixels; 24.6 mm square imager)
  - Common device compatible with both in-plane and off-plane grating readouts
  - Radiation damage testing of Gen1 devices, 12/02
- NASA ROSS2002 Proposal for EDCCD Research in FY03
  - Thinned EDCCD, with fully-depleted MBE backside
  - <50Å deadlayer (excellent QE down to E_x~100 eV))